CIRCUIT AND METHOD FOR DEMODULATING A SERVO POSITION BURST

Cross-reference to Related Applications

[1]   This application is related to U.S. Patent Application Ser. Nos. _____

5   (Atty. Docket No. 99-S-190 (1678-22-1)) entitled "DATA-STORAGE DISK HAVING

FEW OR NO SPIN-UP WEDGES AND METHOD FOR WRITING SERVO WEDGES

ONTO THE DISK," _____ (Atty. Docket No.01-S-044 (1678-22-2)) entitled

"CIRCUIT AND METHOD FOR DETECTING A SERVO WEDGE ON SPIN UP OF A

DATA-STORAGE DISK", _____ (Atty. Docket No. 01-S-047 (1678-22-3)) entitled

10   "CIRCUIT AND METHOD FOR DETECTING A SPIN-UP WEDGE AND A

CORRESPONDING SERVO WEDGE ON SPIN UP OF A DATA-STORAGE DISK", ____

_____ (Atty. Docket No. 01-S-023 (1678-39)) entitled "A DATA CODE AND

METHOD FOR CODING DATA", _____ (Atty. Docket No. 01-S-045 (1678-48)) entitled

"CIRCUIT AND METHOD FOR DETECTING THE PHASE OF A SERVO SIGNAL", ____

15   _____ (Atty. Docket No. 01-S-054 (1678-49)) entitled "SERVO CIRCUIT

HAVING A SYNCHRONOUS SERVO CHANNEL AND METHOD FOR

SYNCHRONOUSLY RECOVERING SERVO DATA", which were filed on the same day

as the present application and which are incorporated by reference.

Field of the Invention

20   [2]   The invention is related generally to electronic circuits, and more

particularly to a circuit and method for demodulating a read-write-head position burst in

a servo wedge without the need for over sampling or synchronization between the

sample clock and the servo burst. Such a circuit and method often allows the position

25   bursts to have a higher freqency, thus allowing the bursts to occupy less space on a

disk. Furthermore, such a circuit and method often provide more accurate

demodulation of the position burst — and thus often allow a more accurate positioning

of the read-write head — because their accuracy is unaffected by disk jitter or other

events that often degrade the synchronization between the sample clock and the servo

30   signal.

BACKGROUND OF THE INVENTION

[3]   As software applications become larger and more data intensive, disk-drive manufacturers are increasing the data-storage capacities of data-storage disks by increasing the disks' data-storage densities (bits/inch). This increase in storage density typically increases the frequency of the read signal from the read-write head of the disk drive that incorporates such a disk.

[4]   Unfortunately, as discussed in more detail below in conjunction with FIGS. 1 – 5, increasing the density of the servo data, and thus increasing the frequency of the servo signal, may cause a disk drive's head-position circuit to improperly position the read-write head over a selected data track. A servo circuit typically heavily over samples or uses fewer synchronized samples of the servo signal to calculate the amplitudes of read-write head position bursts that are stored on the disk. Using these burst amplitudes, the disk drive calculates a head-position error signal, which the head-position circuit uses to position the head over the selected data track. But if the frequency of the servo signal is too high, the servo circuit may be unable to generate enough samples for over sampling or maintain synchronization between the sample clock and the servo burst, and thus may calculate inaccurate values for the burst amplitudes. Consequently, these inaccurate values may cause the disk drive to calculate an erroneous value for the head-position error signal, and thus may cause the head-position circuit to improperly position the head over the selected data track.

[5]   FIG. 1 is a plan view of a conventional disk drive 10, which includes a magnetic data-storage disk 12, a read-write head 14, an arm 16, and a voice-coil motor 18. The disk 12 is partitioned into a number — here eight — of disk sectors 20a-20h, and includes a number — typically in the tens or hundreds of thousands — of concentric data tracks 22a-22n. Readable-writable application data is stored in respective data sectors (not shown) within each track 22. Under the control of the disk drive's head-position circuit (not shown in FIG. 1), the motor 18 moves the arm 16 to center the head 14 over a selected track 22.

[6]   Referring to FIG. 2, conventional data servo wedges 24 — only servo wedges 24a - 24c are shown for clarity — include servo data that allows the
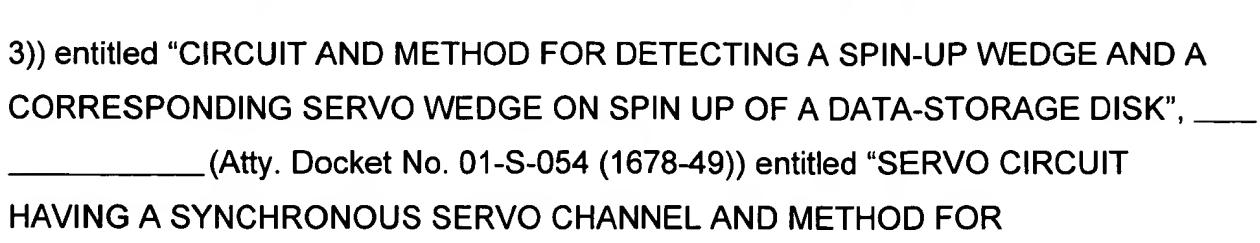
head-position circuit (not shown in **FIG. 2**) of the disk drive **10** (**FIG. 1**) to accurately position the read-write head **14** (**FIG. 1**) during a data read or write operation. The servo wedges **24** are located within each track **22** at the beginning — the disk **12** spins counterclockwise in this example — of each disk sector **20**. Each servo wedge **24**

5   includes respective servo data that indentifies the location (track **22** and sector **20**) of the servo wedge. Thus, the head-position circuit uses this servo data to position the head **14** over the track **22** selected to be read from or written to. The manufacturer of the disk drive **10** typically writes the servo wedges **24** onto the disk **12** before shipping the disk drive to a customer; neither the disk drive nor the customer alters the servo

10   wedges **24** thereafter. Servo wedges like the servo wedges **24** are further discussed below in conjunction with **FIG. 3** and in commonly owned U.S. Patent App. Ser. No. 09/783,801, filed February 14, 2001, entitled "VITERBI DETECTOR AND METHOD FOR RECOVERING A BINARY SEQUENCE FROM A READ SIGNAL," which is incorporated by reference.

15   **[7]**   **FIG. 3** is a diagram of the servo wedge **24a** of **FIG. 2**, the other servo wedges **24** being similar. Write splices **30a** and **30b** respectively separate the servo wedge **24a** from adjacent data sectors (not shown). An optional servo address mark (SAM) **32** indicates to the head-position circuit (not shown in **FIG. 3**) that the read-write head **14** (**FIG. 1**) is at the beginning of the servo wedge **24a**. A servo preamble **34**

20   allows the servo circuit (not shown in **FIG. 3**) of the disk drive **10** (**FIG. 1**) to synchronize the sample clock to the servo signal (**FIG. 5**), and a servo synchronization mark (SSM) **36** identifies the beginning of a head-location identifier **38**. Once the beginning of the identifier 38 is identified, a disk-drive controller (**FIG. 9**) can determine the beginnings of head-position bursts A – N by counting cycles of the sample clock. The

25   preamble **34** and SSM **36** are discussed in commonly owned U.S. Patent application numbers _____ (Atty. Docket No. 99-S-190 (1678-22-1)) entitled "DATA-STORAGE DISK HAVING FEW OR NO SPIN-UP WEDGES AND METHOD FOR WRITING SERVO WEDGES ONTO THE DISK," _____ (Atty. Docket No.01-S-044 (1678-22-2)) entitled "CIRCUIT AND METHOD FOR DETECTING A SERVO WEDGE ON SPIN

30   UP OF A DATA-STORAGE DISK", _____ (Atty. Docket No. 01-S-047 (1678-22-

3)) entitled "CIRCUIT AND METHOD FOR DETECTING A SPIN-UP WEDGE AND A CORRESPONDING SERVO WEDGE ON SPIN UP OF A DATA-STORAGE DISK", ____ _____(Atty. Docket No. 01-S-054 (1678-49)) entitled "SERVO CIRCUIT HAVING A SYNCHRONOUS SERVO CHANNEL AND METHOD FOR

5 SYNCHRONOUSLY RECOVERING SERVO DATA", which are incorporated by reference. The location identifier 38 allows the head-position circuit to coarsely determine and adjust the position of the head 14 with respect to the surface of the disk 12 (FIG. 1). More specifically, the location identifier 38 includes a sector identifier 40 and a track identifier 42, which respectively identify the disk sector 20 and the data track

10 22 — here the sector 20a and the track 22a — that contain the servo wedge 24a. Because the head 14 may read the location identifier 38 even if the head is not centered over the track 24a, the servo wedge 24a also includes the head-position bursts A - N, which allow the head-position circuit to finely determine and adjust the position of the head 14 as discussed below in conjunction with FIGS. 4 and 5.

15 [8]   FIG. 4 is a close-up view of a portion 48 of the disk 10 (FIG. 1), the portion 48 including four sections 50A – 50D of head-position bursts A – D, respectively. More specifically, the portion 48 includes adjacent tracks 22_n – 22_{n+7}, the illustrated portions of which include the servo wedges 24 (FIG. 3), burst sections 50A – 50D, and write splices 30 and/or application data. Each of the bursts in sections 50A – 50D is

20 two tracks wide in a radial direction and is staggered with respect to the tracks 22 such that the boundaries 52 and 54 between adjacent bursts in the same section are aligned with the centers of respective tracks 22. For example, the boundary 52_{i+1} between adjacent bursts A_j and A_{j+1} and B_j and B_{j+1} is aligned with the center of the track 22_{n+2}. Furthermore, the bursts in each section 50A – 50D alternate between a logic 1

25 (represented by an "X") value and a logic 0 (represented by a blank, i.e., the absence of an "X") value, and the values of the bursts in sections 50A and 50C are opposite to the values of the adjacent bursts in sections 50B and 50D, respectively. For example, bursts A_j, A_{j+1}, and A_{j+2} in section A have alternating values 0, 1, 0, respectively, and adjacent bursts A_{j+1} and B_{j+1} have opposite values logic 1 and logic 0, respectively. In

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one example, logic 1 represents a nonzero voltage level, and logic 0 represents a zero voltage level.

[9]   In operation, the head-position circuit (not shown in **FIG. 4**) uses the relative magnitudes of diagonally adjacent bursts in sections **50A** and **50B** or in

5   sections **50C** and **50D** to center the head **14** (**FIG. 1**) over a desired track. For example, assume that the head-position circuit is to center the head **14** over the track 22_{n+2}. First using a conventional technique omitted here for clarity, the head-position circuit coarsely positions the head **14** over or near the track 22_{n+2} and reads the track identifier **42** (**FIG. 3**) that the head **14** is over. If the read track identifer belongs to the

10   track 22_{n+2}, then the head-position circuit determines that the head **14** is close enough to the track 22_{n+2} to proceed with the fine positioning of the head. Because the boundary 52_{i+1} is aligned with the center of the track 22_{n+2}, to center the head **14** the disk drive **10** (**FIG. 1**) reads and compares the magnitudes of the diagonally adjacent bursts A_{j+1} and B_j and calculates a position-error signal proportional to the difference

15   between the magnitudes of A_{j+1} and B_j. The head-position circuit uses this error signal to move the head **14** toward, and ideally over, the center of the track 22_{n+2}.

[10]   More specifically, the disk drive **10** (**FIG. 1**) and the head-position circuit (not shown in **FIG. 4**) operate according to Table I to center the head **14** (**FIG. 1**) over the track 22_{n+2}, where Mag A equals the read-voltage level, *i.e.*, magnitude, of A_{j+1}, and

20   Mag B equals the read-voltage level, *i.e.*, magnitude, of B_j (A_j and B_{j+1}, which are logic 0, have zero voltage levels in this example):
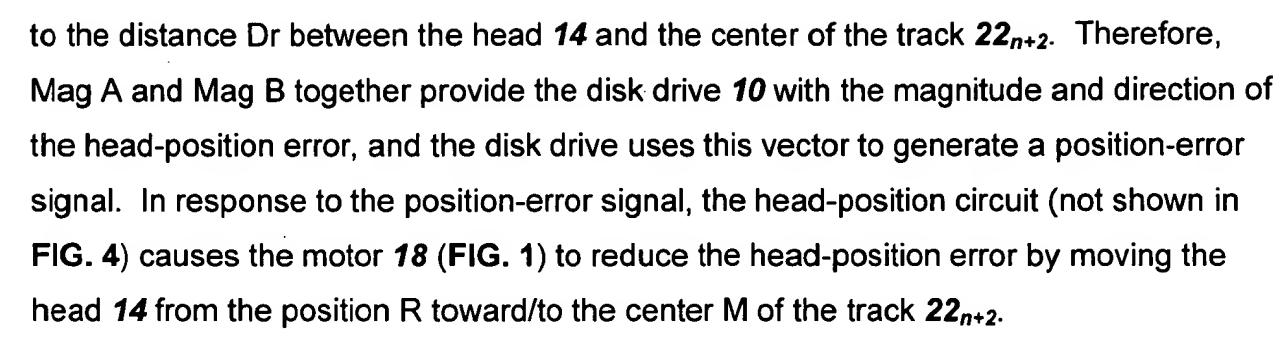
5

Table I

First Scenario	Mag A > Mag B	To center the head over track $22n+2$ if the head 14 is not centered over the track 22_{n+2} and is closer to the track 22_{n+3}, the head-position circuit needs to moves the head 14 toward/to the center of the track 22_{n+2} in a direction toward the center (bottom of **FIG. 4**) of the disk 10.
Second Scenario	Mag A = Mag B	The head 14 is centered over the track 22_{n+2}. Therefore, the head-position circuit does not need to move the head 14 for track $22n+2$ centering..
Third Scenario	Mag A < Mag B	The head 14 is not centered over the track 22_{n+2}, and is closer to the track 22_{n+1}. Therefore, the head-position circuit moves the head 14 toward/to the center of the track 22_{n+2} in a direction toward the center of the disk 10.

[11]   To illustrate the first scenario, assume that after coarse positioning, the head 14 is over the track 22_{n+3} at a position R, which is a radial distance +Dr from the

5   center M of the track 22_{n+2} — the center M is aligned with the boundary 52_{i+1}. When the disk 10 (**FIG. 1**) rotates such that the head 14 is aligned with the burst section $50A$, the burst A_{j+1} is directly beneath the head such that the servo-signal voltage level, Mag A, has a maximum value. Conversely, when the disk 10 rotates such that the head 14 is aligned with the burst section $50B$, the head is radially spaced +Dr from the

10   boundary 52_{i+1}, and thus from the burst B_j, such that the servo-signal voltage level, Mag B, has a nonmaximum value that is less than Mag A. Because Mag A > Mag B, the disk drive 10 "knows" the direction of the head-position error, *i.e.*, that the head 14 is closer to the track 22_{n+3} than to the track 22_{n+1}. Furthermore, |Mag A – Mag B| is proportional

to the distance Dr between the head **14** and the center of the track 22_{n+2}. Therefore, Mag A and Mag B together provide the disk drive **10** with the magnitude and direction of the head-position error, and the disk drive uses this vector to generate a position-error signal. In response to the position-error signal, the head-position circuit (not shown in

5 **FIG. 4**) causes the motor **18** (**FIG. 1**) to reduce the head-position error by moving the head **14** from the position R toward/to the center M of the track 22_{n+2}.

[12]   To illustrate the second scenario, assume that after coarse positioning, the head **14** is over the center M of the track 22_{n+2}. When the head **14** is over the burst sections **50A** and **50B**, it is aligned with the boundary 52_{i+1}. Because the boundary

10   52_{i+1} is equidistant from the bursts A_{j+1} and B_j in a radial direction, Mag A = Mag B. Because Mag A = Mag B, the disk drive **10** "knows" that the head **14** is centered over the track 22_{n+2}, and thus "knows" that no position correction is necessary. This follows from |Mag A − Mag B| = 0, which indicates that the error distance is zero.

[13]   To illustrate the third scenario, assume that after coarse positioning, the

15   head **14** is over the track 22_{n+1} at a position Q, which is a radial distance -Dq from the center M of the track 22_{n+2} — "-" indicates that Dq and Dr are in opposite directions from M. Therefore, because Mag B > Mag A, the disk drive **10** "knows" that the head **14** is closer to the track 22_{n+1} than to the track 22_{n+3}, and thus generates a corresponding position-error signal. In response to this position-error signal, the head-position circuit

20   that causes the motor **18** to move the head **14** from Q toward/to the center M of the track 22_{n+2}.

[14]   Although the servo-wedge portions (to the left of the bursts **50A – 50D**) of the tracks **22** are shown as having the same widths as the corresponding data-sector portions (to the right of the bursts **50A – 50D**) portions, these portions may have

25   different widths. Where the widths are different, the boundaries **52** and **54** are aligned with the centers of the data-sector portions to accurately read the application data.

[15]   **FIG. 5** is a plot of a sinusoidal servo signal that the head **14** (**FIG. 1**) generates while reading a head-position burst, and a sample clock that is not synchronized to the burst sinusoid.
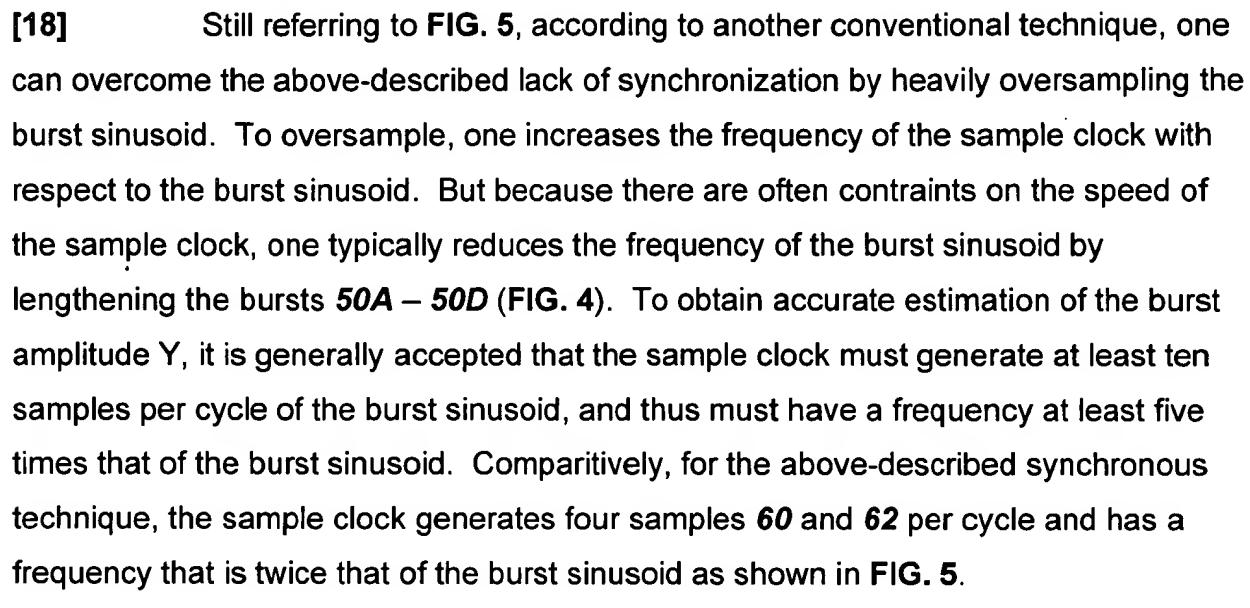
[16]   According to one conventional technique, the servo circuit (not shown in **FIG. 5**) synchronizes the sample clock to the servo signal as the head **14** reads the preamble **34** (**FIG. 3**). Typically, this preamble servo signal (not shown) is a sinusoid similar or identical to the burst sinusoid, and the servo circuit aligns the edges of the sample clock to the peaks and zero crossings of the preamble sinusoid. For example, the servo circuit may align the rising edges of the servo clock with the peaks and the falling edges with the zero crossings. Unfortunately, by the time that the head **14** is over the position-burst sections **50A – 50D** (**FIG. 4**), phenomena such as noise and disk jitter may cause the edges of the sample clock to become offset from the peaks and zero crossings of the burst sinusoid. For example the rising and falling edges of the sample clock may respectively lead the peaks and zero crossings of the burst sinusoid by a nonzero angle α, where it is desired that α equal zero.

[17]   Unfortunately, the lack of synchronization between the sample clock and the burst sinusoid may cause the head-position circuit (not shown in **FIG. 5**) to improperly position the head **14** over the selected track **22** (**FIG. 4**) during the fine positioning of the head. Typically, the peak voltage level Y of the burst sinusoid is the magnitude (*e.g.*, Mag A or Mag B of **FIG. 4**) of the postion burst. In **FIG. 4** for example, |Y| > 0 represents a logic 1 (represented by an "X") and Y= 0 (DC signal) represents a logic 0 (represented by the absence of "X"). Furthermore, the accuracy of the algorithm that the disk drive **10** (**FIG. 1**) uses to demodulate, *i.e.*, calculate the magnitudes of, the position bursts is often proportional to the level of synchronization between the sample clock and the burst sinusoid. For example, assuming perfect synchronization, the samples **60** taken at the rising edges of the sample clock are of the burst-sinusoid peaks, and thus equal Y. Therefore, a simple algorithm averages a number of the samples **60** to filter out noise and calculates the burst magnitude equal to this average. But if the clock and burst sinusoid are imperfectly aligned as shown, then, ignoring noise and jitter, this algorithm yields an incorrect burst magnitude $Y\cos\alpha$ instead of the correct burst magnitude Y. This incorrect burst magnitude may cause the disk drive **10** to calculate an inacccurate position-error signal, which may cause the motor **18** (**FIG. 1**) to move the head **14** to an undesired position.

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[18] Still referring to **FIG. 5**, according to another conventional technique, one can overcome the above-described lack of synchronization by heavily oversampling the burst sinusoid. To oversample, one increases the frequency of the sample clock with respect to the burst sinusoid. But because there are often contraints on the speed of

5 the sample clock, one typically reduces the frequency of the burst sinusoid by lengthening the bursts **50A – 50D** (**FIG. 4**). To obtain accurate estimation of the burst amplitude Y, it is generally accepted that the sample clock must generate at least ten samples per cycle of the burst sinusoid, and thus must have a frequency at least five times that of the burst sinusoid. Comparitively, for the above-described synchronous

10 technique, the sample clock generates four samples **60** and **62** per cycle and has a frequency that is twice that of the burst sinusoid as shown in **FIG. 5**.

[19] Unfortunately, although heavily oversampling allows one to calculate the burst amplitude Y with an unsynchronized sampling clock, it typically requires more disk space due to the above-described lengthening of the position bursts **50A – 50D**

15 (**FIG. 4**).

SUMMARY OF THE INVENTION

[20] In accordance with an embodiment of the invention, a circuit receives fewer than ten samples per cycle of a position burst and calculates the burst magnitude from the samples such that the accuracy of the burst magnitude is independent of the

20 timing of the samples with respect to the burst.

[21] By using an algorithm that does not require heavy over sampling — for purposes of this application, heavy over sampling is a sampling rate more than four samples per cycle — and that is independent of the level of synchronization between

25 the sample clock and the position bursts, such a circuit often allows shorter position bursts than a heavy-over-sampling circuit allows and calculates the burst magnitudes and the head-position-error signal more accurately than a circuit that uses a timing-dependent algorithm.

BRIEF DESCRIPTION OF THE DRAWINGS

[22]   **FIG. 1** is a plan view of a conventional disk drive.

[23]   **FIG. 2** is a close-up view of some tracks and servo wedges on the disk

of **FIG. 1**.

[24]   **FIG. 3** is a diagram of a servo wedge of **FIG. 2**.

[25]   **FIG. 4** is a close-up view of some tracks and position bursts on the disk

of **FIG. 1**.

[26]   **FIG. 5** is a plot of a conventional burst sinusoid and a conventional sample

clock that is not synchronized to the burst sinusoid.

[27]   **FIG. 6** is a block diagram of a position-burst demodulator according to an

embodiment of the invention.

[28]   **FIG. 7** is a phase diagram used to explain how the demodulator of **FIG. 6**

calculates the magnitude of a position burst according to an embodiment of the

invention.

[29]   **FIG. 8** is a block diagram of a servo circuit that incorporates the

position-burst demodulator of **FIG. 6** according to an embodiment of the invention.

[30]   **FIG. 9** is a block diagram of a disk-drive system that incorporates the

servo circuit of **FIG. 8** according to an embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[31]   **FIG. 6** is a block diagram of a position-burst demodulator *70* according to

an embodiment of the invention. As discussed below in conjunction with **FIG. 7**, the

circuit uses a variation of a known trigonometric identity to calculate the magnitude of a

position burst (**FIGS. 4** and **5**) independently of the synchronization, or lack thereof,

between the sample clock (**FIG. 5**) and the postion burst. In the embodiment discussed

in conjunction with **FIG. 6**, the demodulator *70* is part of a servo circuit (**FIG. 8**) and

provides a head-position-error signal to a head-position circuit (**FIG. 9**). Alternatively,

the demodulator *70* may be part of the head-position circuit.

[32]   **FIG. 7** is a phase diagram of a positive half period of the burst sinusoid of **FIG. 5**, and illustrates how the position-burst demodulator **70** of **FIG. 6** calculates a synchronization-independent value for the magnitude Y of the burst sinusoid. Specifically, samples **90** and **92** are 90° apart. Therefore, one can calculate the

5 amplitude Y according to the following equations, which follow from the well-known trigonemetric identity $Sin^2\beta + Cos^2\beta = 1$:

(1) $(YSin\beta)^2 + (YCos\beta)^2 = Y^2Sin^2\beta + Y^2Cos^2\beta = Y^2(Sin^2\beta + Cos^2\beta) = Y^2$

(2)   Sample **90** = $YSin\beta_2$

10 (3)   Sample **92** = $YCos\beta_2$

(4) Y^2 = (sample **90**)^2 + (sample **92**)^2

$$(5) \qquad Y = \sqrt{(sample\,90)^2 + (sample\,92)^2}$$

Further details of this identity are discussed in commonly owned U.S. Patent App. Ser. No. 09/503,949, filed February 14, 2000, entitled "A CIRCUIT AND METHOD FOR CONTROLLING THE GAIN OF AN AMPLIFIER BASED ON THE SUM OF SAMPLES

15 OF THE AMPLIFIED SIGNAL", and U.S. Patent App. Ser. No. 09/503,399, filed February 14, 2000, entitled "A CIRCUIT AND METHOD FOR CONTROLLING THE GAIN OF AN AMPLIFIER", which are incorporated by reference.

[33]   Referring again to **FIG. 6**, in one embodiment the demodulator **70**

20 improves upon the above-described trigonometric identity by effectively averaging the samples of the burst sinusoid of **FIGS. 5** and **7** to filter out noise. For example purposes, the operation of the demodulator **70** is described where the head-position circuit (**FIG. 9**) is attempting to center the head **14** (**FIGS. 1** and **9**) over the track 22_{n+2} (**FIG. 4**), it being understood that the operation of the demodulator **70** is similar when

25 the head-position circuit attempts to center the head over another track.

[34]   More specifically, referring to **FIGS. 4 - 6**, an adder **72a** sums the magnitudes of a number — for example eight — of even samples **60** of the position burst A_{j+1} to generate a sum E, and an adder **72b** sums the magnitudes of the same number of odd samples **62** of the same postion burst to generate a sum O. In one

embodiment, the adders **72a** and **72b** respectively generate the sums E and O by summing the negative of every other sample. For example, the even sample **60a** is positive, but the next even sample **60b** is negative. Therefore, the adder **72a** sums the samples **60a** and **60c**, which are positive values, with the negatives of the

5   samples **60b** and **60d**, these negatives also being positive values (the negative of a negative is a positive). Likewise, the adder **72b** sums the samples **62a** and **62c** with the negatives of the samples **62b** and **62d**. Although one could generate E equal to a single sample **60** and O equal to a single sample **62**, summing multiple samples **60** and **62** to respectively generate E and O averages out noise that may contaminate the burst

10   sinusoid.

[35]   The functions of the adders **72a** and **72b** is represented by the following equations:

(6)   E = (sample **60a** – sample **60b**) + (sample **60c** – sample **60d**) . . .

(7)   O = (sample **62a** – sample **62b**) + (sample **62c** – sample **62d**) . . .

15   [36]   Next, multipliers **74a** and **74b** respectively square E and O and a summer **76** sums E^2 and O^2 according to equation (4), where E effectively corresponds to "sample **90**" and O effectively corresponds to "sample **92**".

[37]   Then, a root circuit **78** takes the square root of $E^2 + O^2$ to generate the magnitude Mag A of the burst A_{j+1}, and stores Mag A in a first memory **80a**.

20   [38]   Next, the demodulator **70** calculates the magnitude Mag B of the burst **Bj** in a similar manner and stores Mag B in a second memory **80b**.

[39]   Then, a subtractor **82** calculates the head-position-error signal equal to Mag B – Mag A. The polarity (+ or -) of the signal indicates the direction of the error, and the value |Mag B - Mag A| indicates the magnitude of the error. Using the error

25   signal, the head-position circuit (**FIG. 9**) finely postions the head **14** as discussed above in conjunction with **FIG. 4**. In other embodiments, however, the subtractor **82** may calculate the error signal equal to Mag A – Mag B, or the demodulator **70** or head-position circuit may further process the error signal before using it to finely position the head **14**.

[40]   Although the demodulator **70** is described as including respective circuit blocks **72a** – **80b**, in other embodiments the demodulator may include a processor or logic circuit programmed to implement the above-described algorithm. Furthermore, the demodulator **70** may use other algorithms to calculate E^2, O^2, and MAG A and MAG B.

5   For example, the circuit **70** can square an even sample **60** to generate E^2, square the next odd sample **62** to generate O^2, take the square root of $E^2 + O^2$, and sum the resulting square roots of $E^2 + O^2$ over a number of samples **60** and **62** to obtain MAG A or MAG B. Other algorithms are contemplated but are omitted for brevity.

[41]   **FIG. 8** is block diagram of a synchronous servo circuit **100**, which includes

10   the position-burst demodulator **70** of **FIG. 6** according to an embodiment of the invention. The circuit **100** includes a gain and filter circuit **102**, which adjusts the gain and filters the servo signal from the read head **14**. An analog-to-digital converter (ADC) **104** receives the sample clock (**FIG. 5**) on a control bus **106** and generates digital samples, such as the samples **60** and **62** (**FIG. 5**), of the analog servo signal from

15   the circuit **102**. A finite-impulse-response (FIR) filter **108** equalizes the samples from the ADC **104**, and timing and gain recovery loops **110** effectively synchronize the sample clock to the servo signal and maintain the gain of the circuit **100** at a desired level. In one embodiment, the circuit **102** and FIR filter **108** equalize the servo signal to a PR4 target, although they may equalize the servo signal to another target such as

20   EPR4. A Viterbi detector **112** recovers servo data such as the location identifier **38** (**FIG. 3**) from the servo-signal samples, and a sync-mark detector **114** recovers the servo sync mark **36** (**FIG. 5**) from the servo signal. If the servo data is encoded, a decoder **116** decodes the recovered servo data and sync mark from the Viterbi and sync mark detectors **112** and **114**, respectively. The position-burst demodulator **70**

25   receives the even and odd samples **60** and **62** (**FIG. 5**) from the FIR **108** and generates the head-position-error signal, and a processor **118** controls the components of the servo circuit **100** via the control bus **106**. A servo-data interface **120** interfaces the decoder **116**, processor **118**, and demodulator **70** to a disk-drive controller (**FIG. 9**).

[42]   Because the demodulator **70** implements a timing-independent algorithm

30   as discussed above, it can calculate the position-error signal without introducing

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additional latency into the algorithm. Specifically, the timing-recovery portion of the loops **110** synchronizes the sample clock to the servo signal by shifting the values of the samples, not by shifting the phase of the sample clock. Therefore, if the demodulator **70** required synchronized samples, it would need to receive them from a point after the

5   timing-loop portion of the loops **110**, which would introduce significant latency into the burst-demodulation calculation. But because the burst-demodulation algorithm is timing independent, the demodulator **70** can receive the potentially unsynchronized burst samples from the FIR **108**, and thus calculate the position-error signal without the latency of the loops **110**.

10   **[43]**   Still referring to **FIG. 8**, the circuit **102**, ADC **104**, FIR **108**, loops **110**, Viterbi detector **112**, decoder **116**, processor **118** and operation of the servo circuit **100** are further discussed in commonly owned patent applications _____ (Atty. Docket No. 99-S-190 (1678-22-1)) entitled "DATA-STORAGE DISK HAVING FEW OR NO SPIN-UP WEDGES AND METHOD FOR WRITING SERVO WEDGES ONTO THE

15   DISK," _____ (Atty. Docket No.01-S-044 (1678-22-2)) entitled "CIRCUIT AND METHOD FOR DETECTING A SERVO WEDGE ON SPIN UP OF A DATA-STORAGE DISK", _____ (Atty. Docket No. 01-S-047 (1678-22-3)) entitled "CIRCUIT AND METHOD FOR DETECTING A SPIN-UP WEDGE AND A CORRESPONDING SERVO WEDGE ON SPIN UP OF A DATA-STORAGE DISK",_____ (Atty. Docket No. 01-S-

20   054 (1678-49)) entitled "SERVO CIRCUIT HAVING A SYNCHRONOUS SERVO CHANNEL AND METHOD FOR SYNCHRONOUSLY RECOVERING SERVO DATA". The timing-recovery loop of the loops **110** is further discussed in commonly owned U.S. Patent App. Ser. No. 09/387,146, filed August 31, 1999, entitled "DIGITAL TIMING RECOVERY USING BAUD RATE SAMPLING", and the gain-recovery loop of the

25   loops **110** and the Viterbi detector **112** are also discussed in commonly owned Patent App. Ser. No. 09/783,801, (Atty. Docket No. 99-S-185 (1678-21)), filed February 14, 2001, entitled "VITERBI DETECTOR AND METHOD FOR RECOVERING A BINARY SEQUENCE FROM A READ SIGNAL," all of which are incorporated by reference. The sync mark detecor **114** is further discussed in commonly owned patent application _____

30   _____ (Atty. Docket No. 01-S-045 (1678-48)) entitled "CIRCUIT AND METHOD

FOR DETECTING THE PHASE OF A SERVO SIGNAL", and the decoder *116* may be constructed to decode servo data that is encoded according to the scheme discussed in commonly owned U.S. Patent App. Ser. Nos. 09/783,801, (Atty. Docket 99-S-185 (1678-21)), filed February 14, 2001, entitled "VITERBI DETECTOR AND METHOD FOR

5 RECOVERING A BINARY SEQUENCE FROM A READ SIGNAL", or the scheme discussed in _____ (Atty. Docket No. 01-S-023 (1678-39)) entitled "A DATA CODE AND METHOD FOR CODING DATA", which are incorporated by reference.
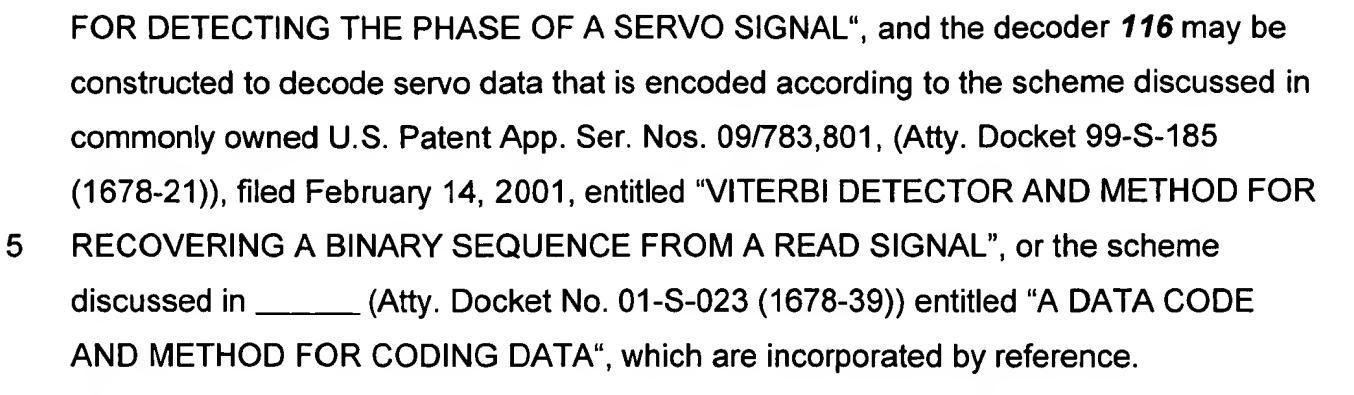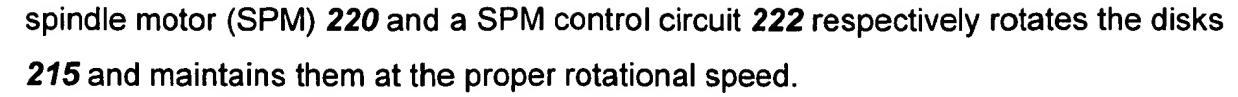
[44] **FIG. 9** is a block diagram of a disk-drive system *200* that incorporates the servo circuit *100* of **FIG. 8** according to an embodiment of the invention, where like

10 numbers reference components common to **FIGS. 1** and **9**. The disk-drive system *200* includes a disk drive *202*, which incorporates the servo circuit *30* of **FIG. 8**. The disk drive *202* includes the read-write head *14*, a write channel *206* for generating and driving the head *14* with a write signal, and a write controller *208* for interfacing the write data to the write channel *206*. The disk drive *202* also includes a read channel *210* for

15 receiving servo and application-data read signals from the head *32* and for recovering data from these read signals, and includes a read controller *212* for organizing the read data. Together, the write and read controllers *208* and *212* compose a disk-drive controller *213*. The read channel *210* includes the servo circuit *30*, which receives the servo signal from the head *14*, recovers the servo data from the servo signal, and

20 provides the recovered servo data to a head-position circuit *214*. The disk drive *202* further includes a storage medium such as one or more disks *215*, each of which may contain data on one or both sides and which may be magnetic, optical, or another type of storage disk. For example, the disks *215* may be similar to the disk *12* of **FIG. 1**. The head *14* writes/reads the data stored on the disk *12*, and is connected to the

25 movable support arm *16*. As discussed above in conjunction with **FIGS. 6-7**, the servo circuit *100* calculates the position-error signal, and, in response to the error signal, the head-position circuit *214* provides a control signal to the voice-coil motor (VCM) *18*, which positionally maintains/radially moves the arm *16* so as to positionally maintain/radially move the head *14* over the desired data tracks on the disks *215*. A

spindle motor (SPM) *220* and a SPM control circuit *222* respectively rotates the disks *215* and maintains them at the proper rotational speed.

[45] The disk-drive system *200* also includes write and read interface adapters *224* and *226* for respectively interfacing the disk-drive controller *213* to a

5 system bus *228*, which is specific to the system used. Typical system busses include ISA, PCI, S-Bus, Nu-Bus, etc. The system *200* typically has other devices, such as a random access memory (RAM) *230* and a central processing unit (CPU) *232* coupled to the bus *228*.

[46] As discussed above, although the burst demodulator *70* (**FIG. 6**) is

10 described as being part of the servo circuit *100*, it may be part of the head-position circuit *214* instead.

[47] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the

15 invention.